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**Reg. no: 19BEC1243**

**Date: 27-09-2021**

**EXPERIMENT NO: 7**

**Design of Logic gates using NMOS, PMOS and Resistor**

**Aim:** To design Logic gates using NMOS, PMOS and Resistor in LTSpice.

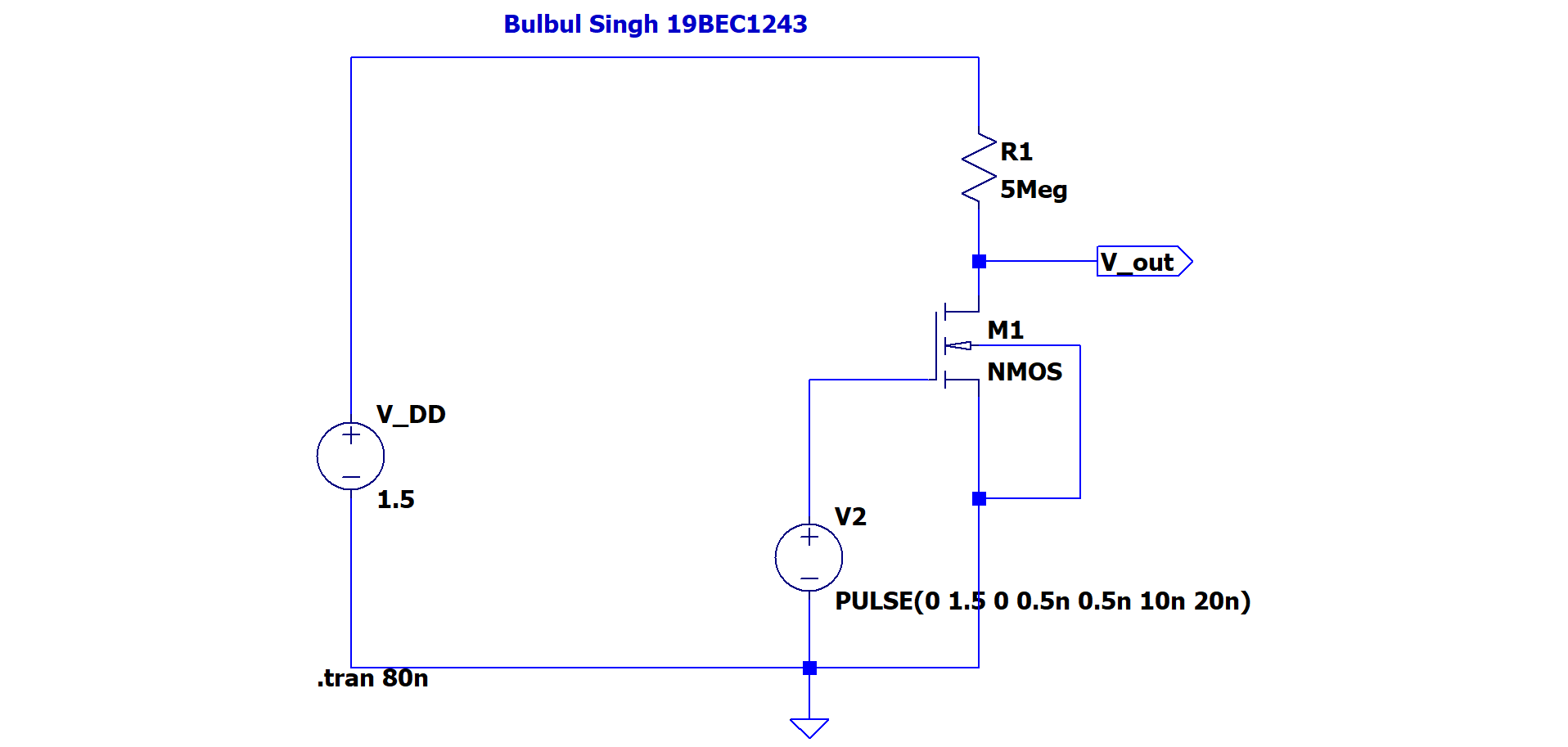
**Software used:** LTSpice

**Components required:** Resistors, voltage source, NMOS, PMOS.

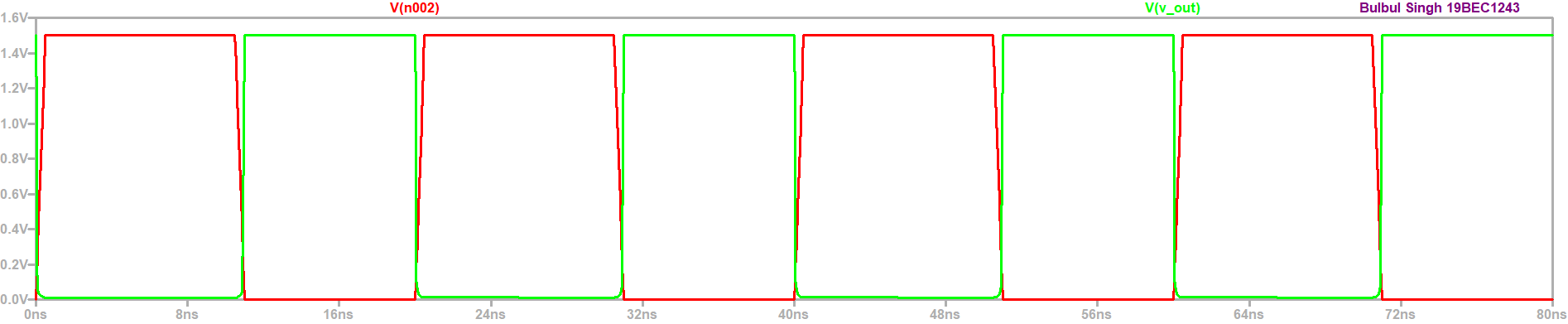
**Task 1:**

**1.1**: **NOT GATE with NMOS**

**Circuit:**



**Output:**

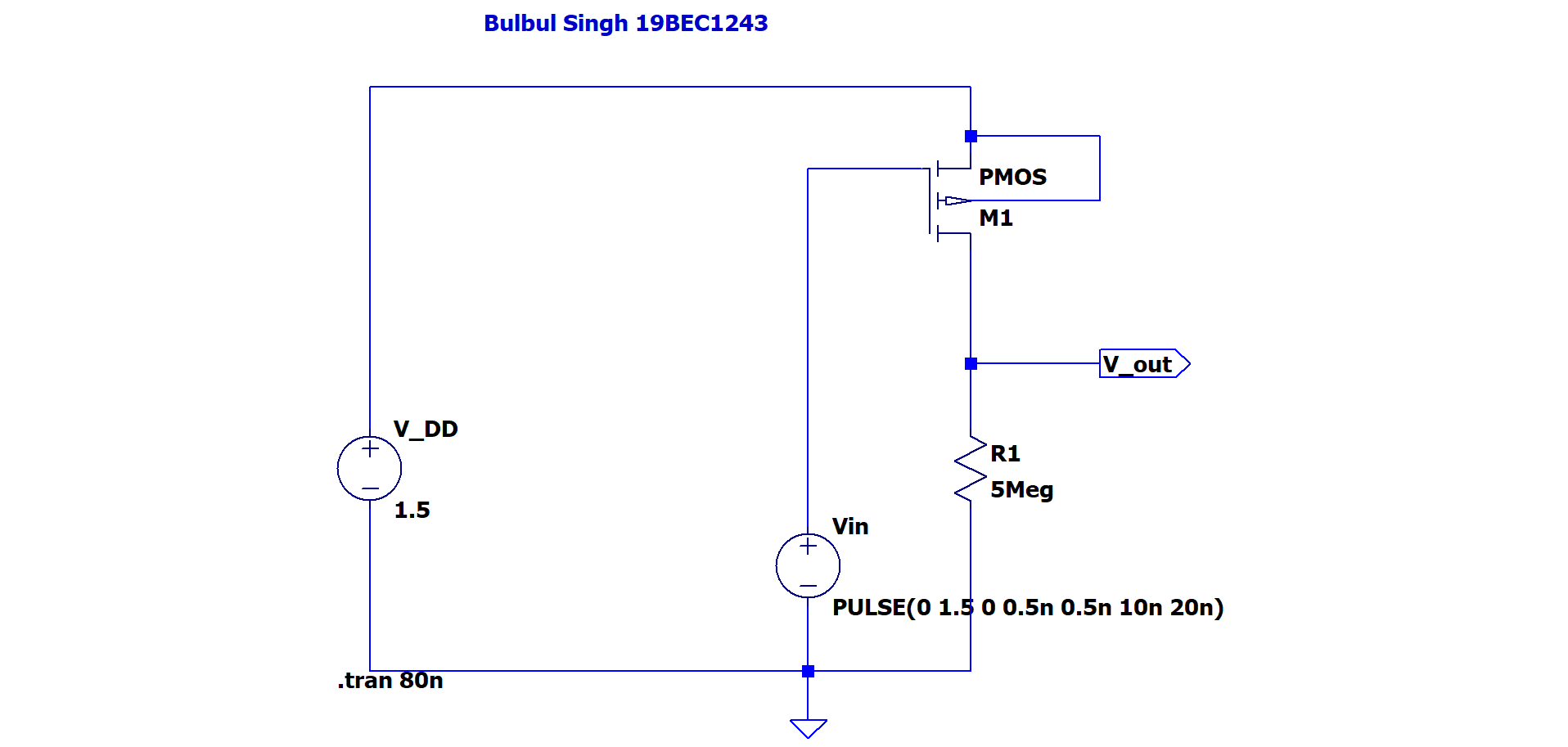
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**Truth Table:**

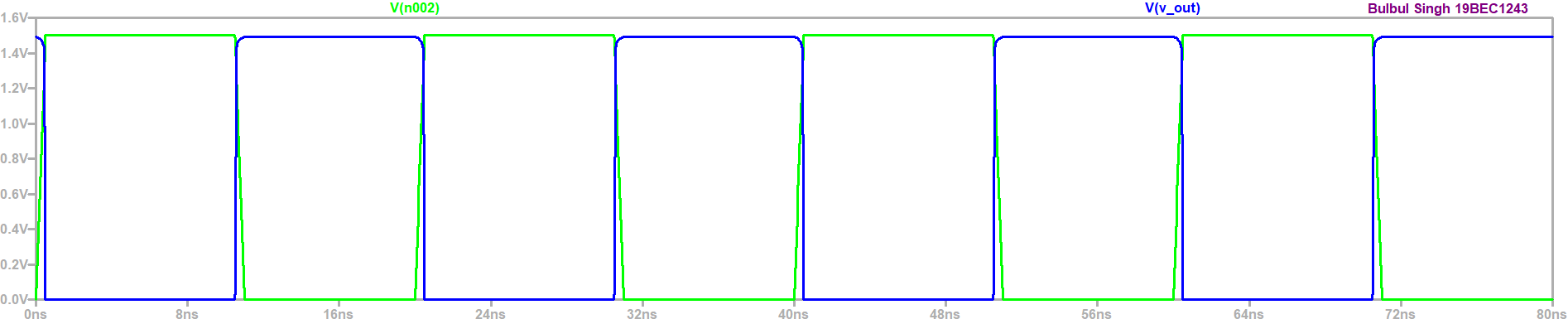
|  |  |
| --- | --- |
| **Vin** | **Vout** |
| 1 | 0 |
| 0 | 1 |

**1.2: NOT GATE with NMOS**

**Circuit:**



**Output:**

****

**Truth Table:**

|  |  |
| --- | --- |
| **Vin** | **Vout** |
| 1 | 0 |
| 0 | 1 |

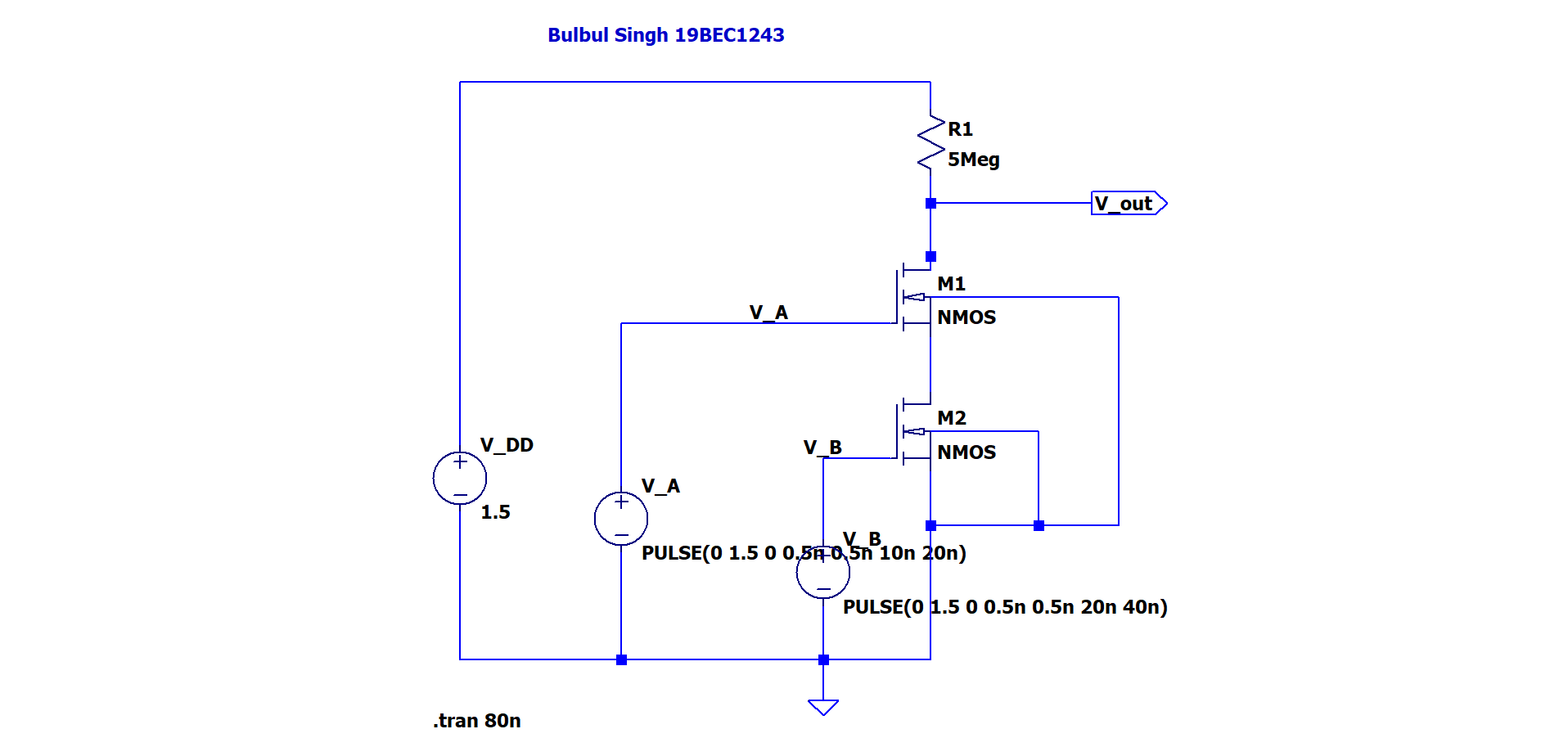
**Conclusion:**

From the graphs of task 1.1 and 1.2 we can observe that when input is low, output is high and when output is low input is high, this shows the functionality of NOT gate and satisfies the truth table.

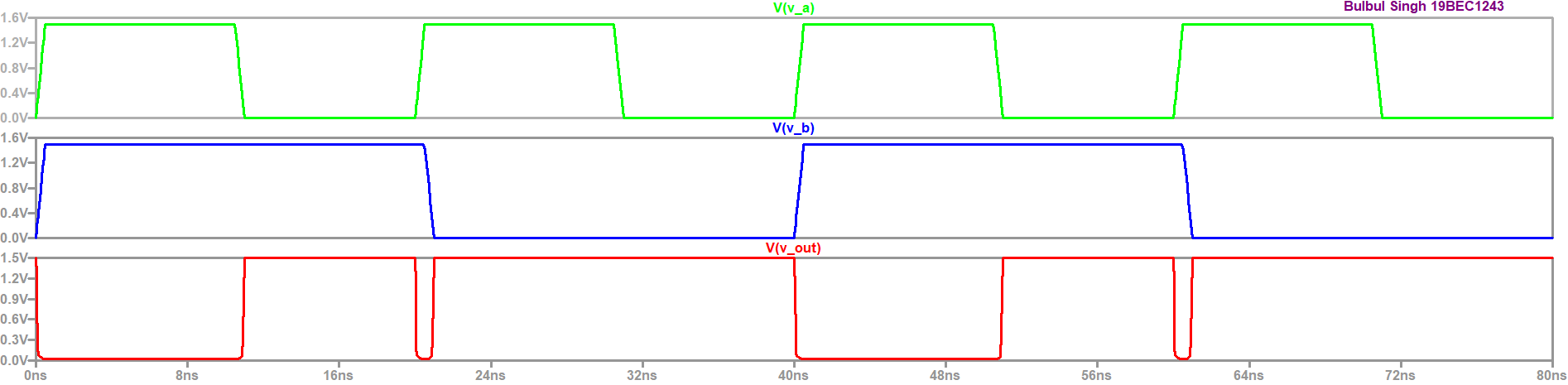
**Task 2:**

**2.1: NAND GATE Using NMOS(NMOS4 symbol)**

**Circuit:**

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**Output:**

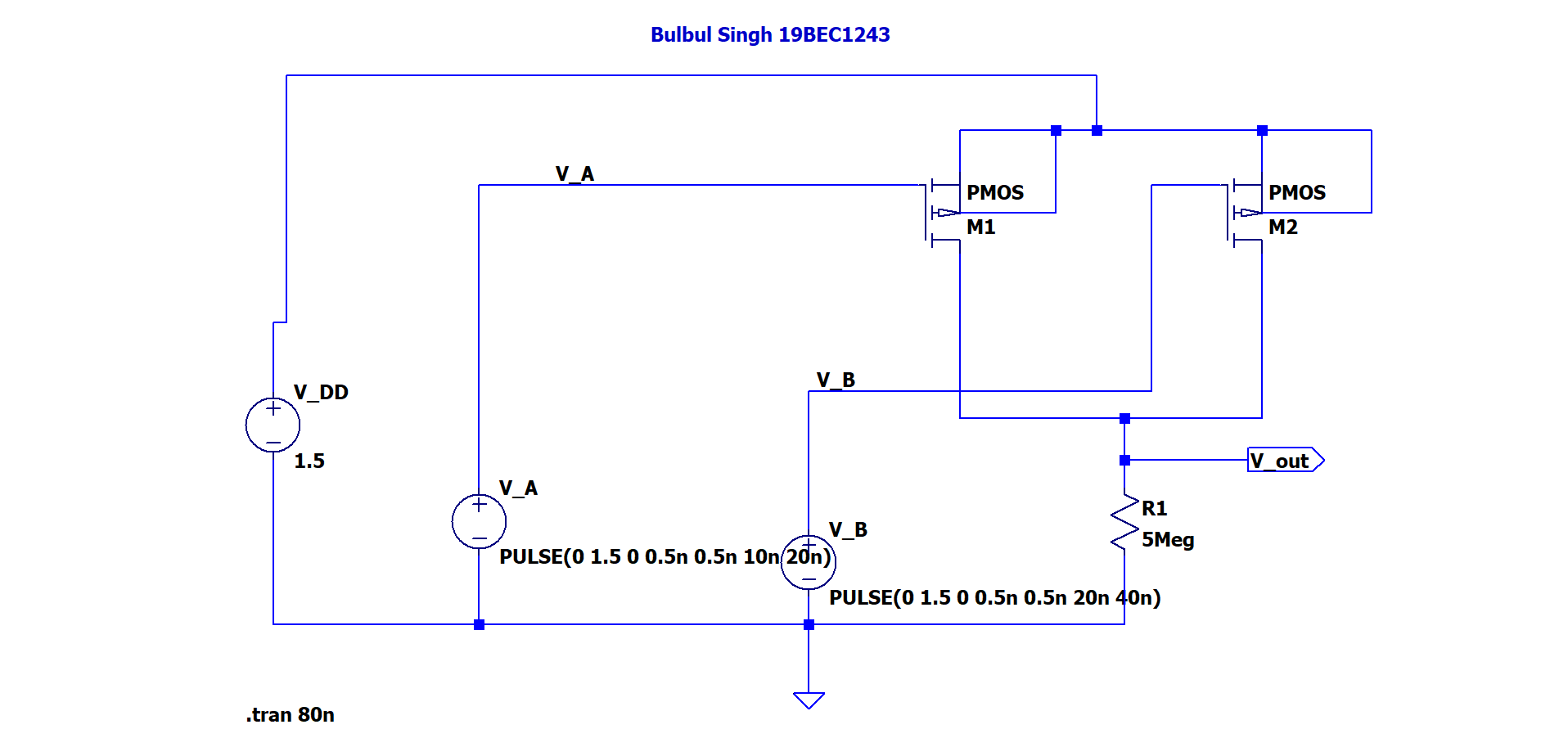


**Truth Table:**

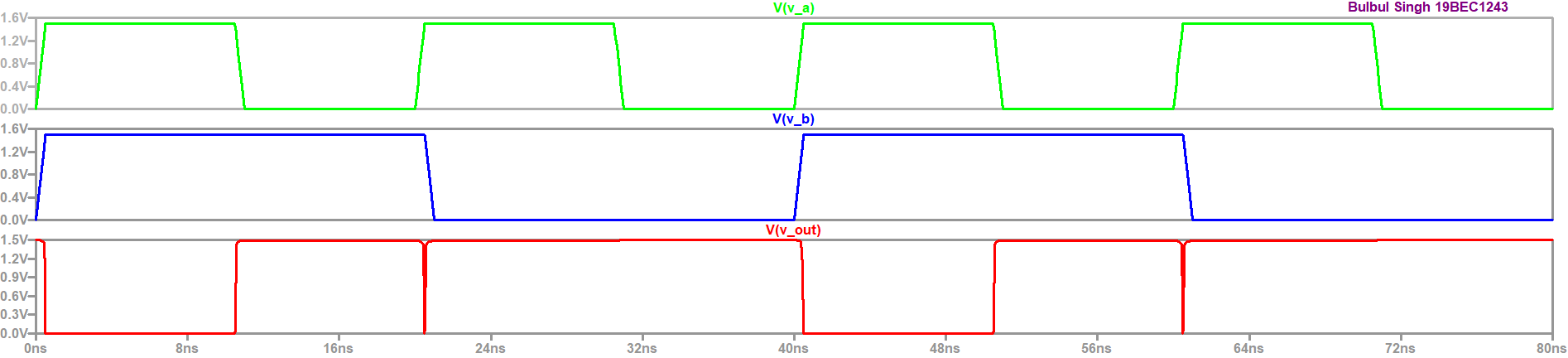
|  |  |  |
| --- | --- | --- |
| **V\_A** | **V\_B** | **V\_out** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**2.2: NAND GATE Using PMOS (PMOS4 symbol)**

**Circuit:**



**Output:**

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**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **V\_A** | **V\_B** | **V\_out** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

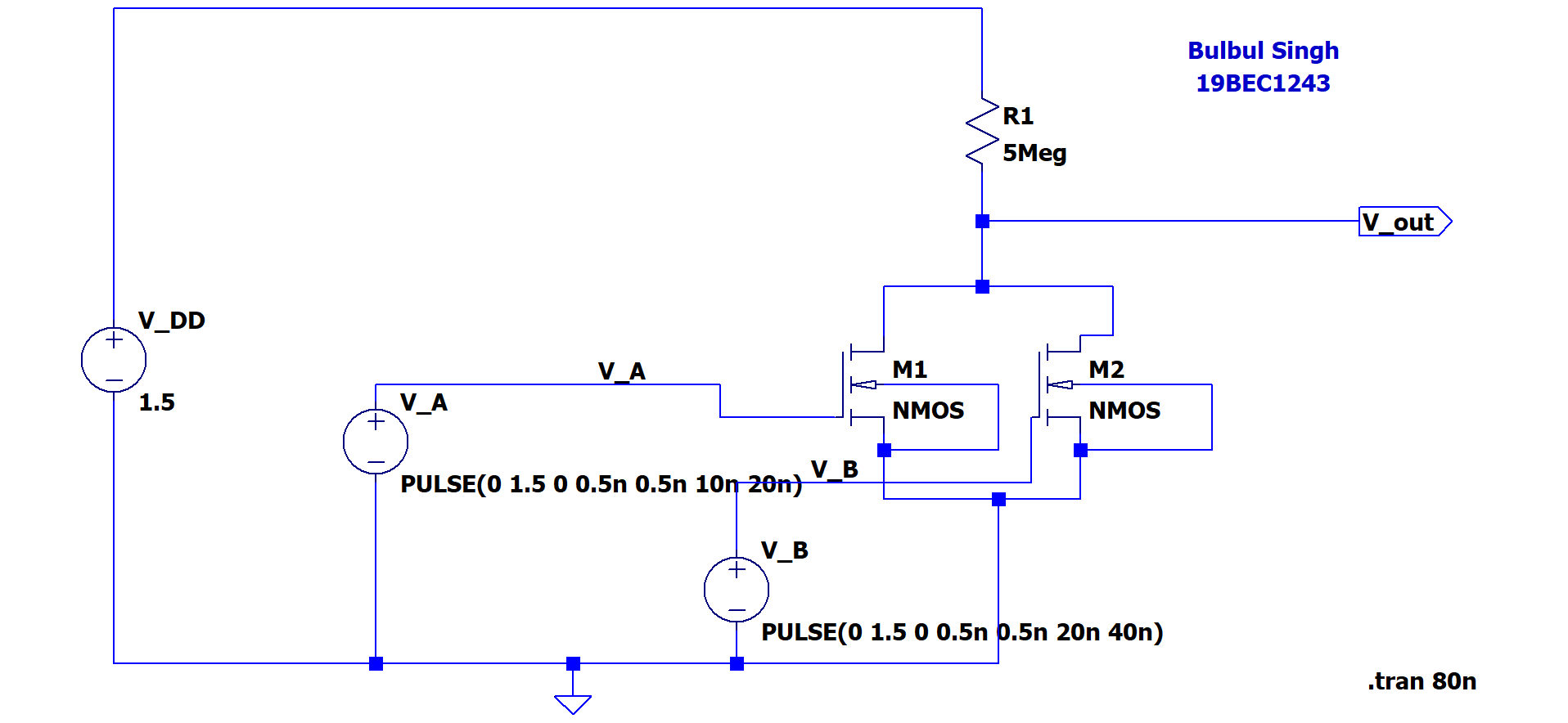
**Conclusion:**

From the graphs of task 2.1 and 2.2 we can observe that when both inputs are high, output is low while in all other cases it is high, this shows the functionality of NAND gate and satisfies the truth table.

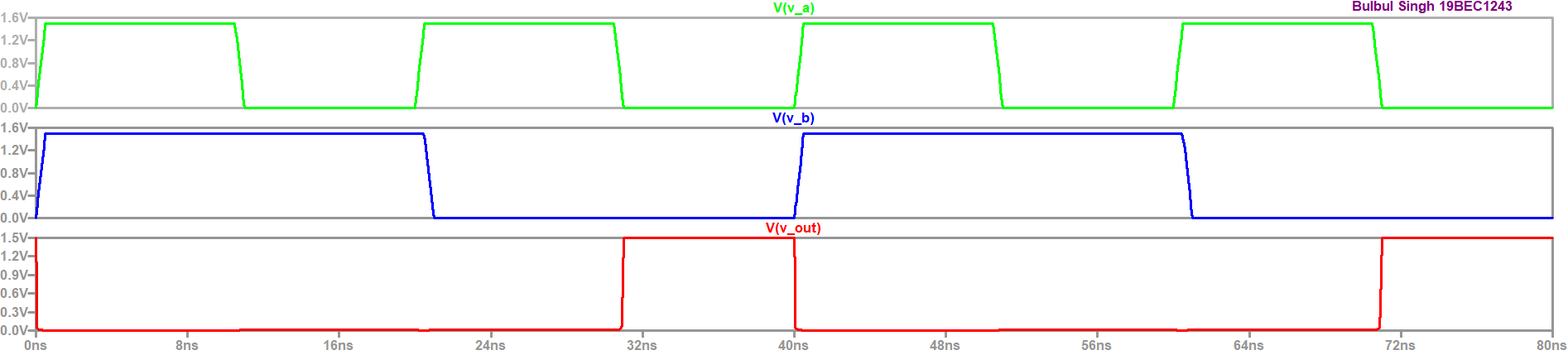
**Task 3:**

**3.1:** **NOR GATE Using NMOS(NMOS4 symbol)**

**Circuit:**

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**Output:**

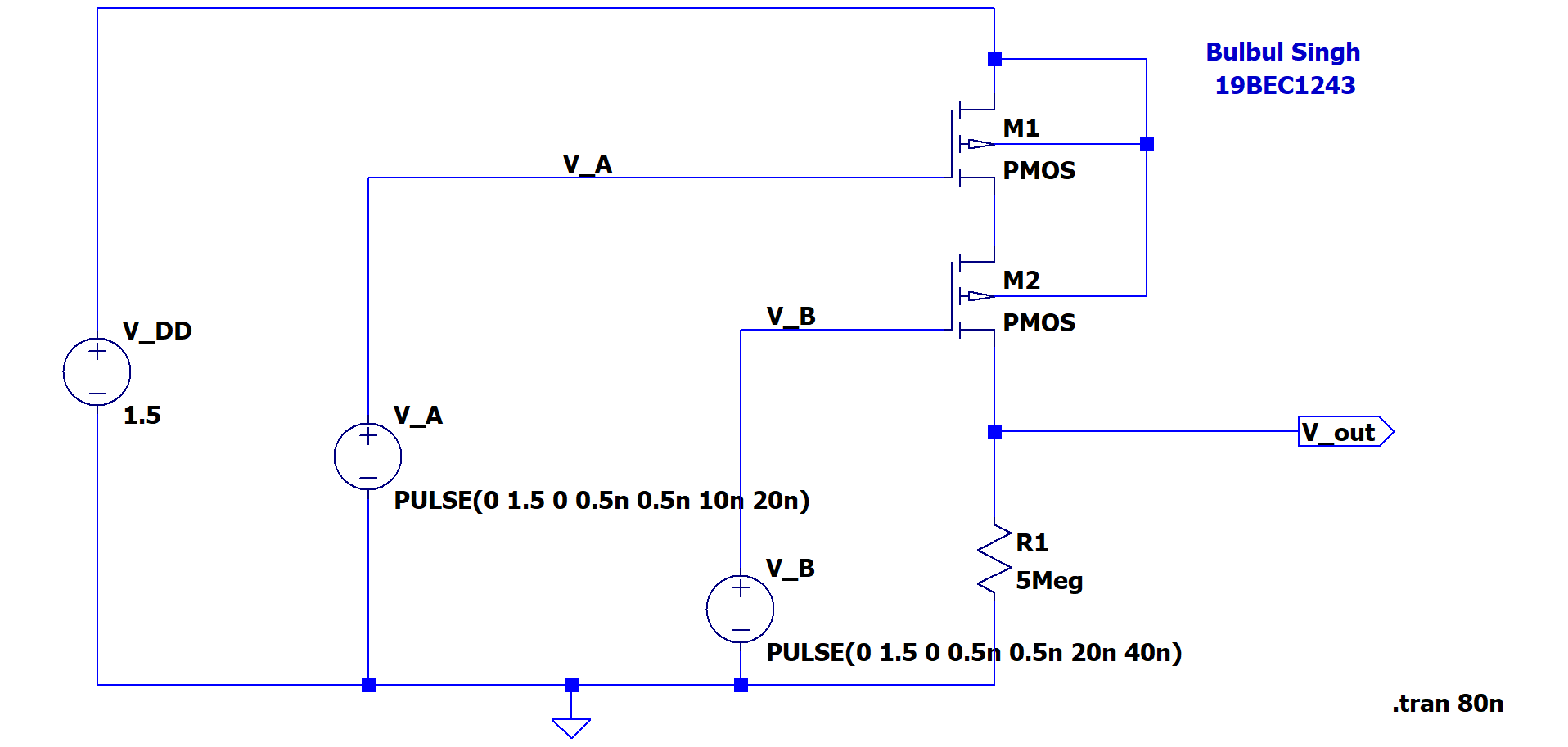
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**Truth Table:**

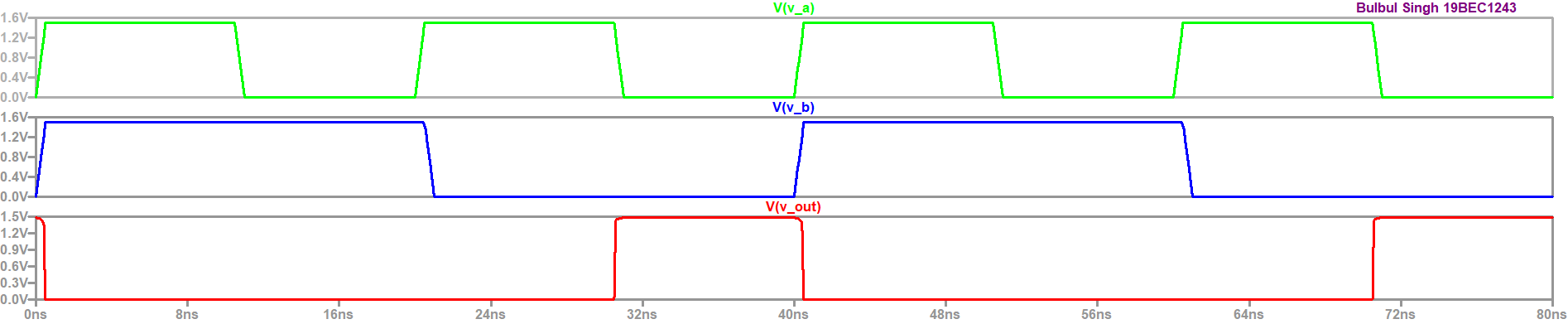
|  |  |  |
| --- | --- | --- |
| **V\_A** | **V\_B** | **V\_out** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**3.2: NOR GATE Using NMOS (NMOS4 symbol)**

**Circuit:**

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**Output:**

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**Truth Table:**

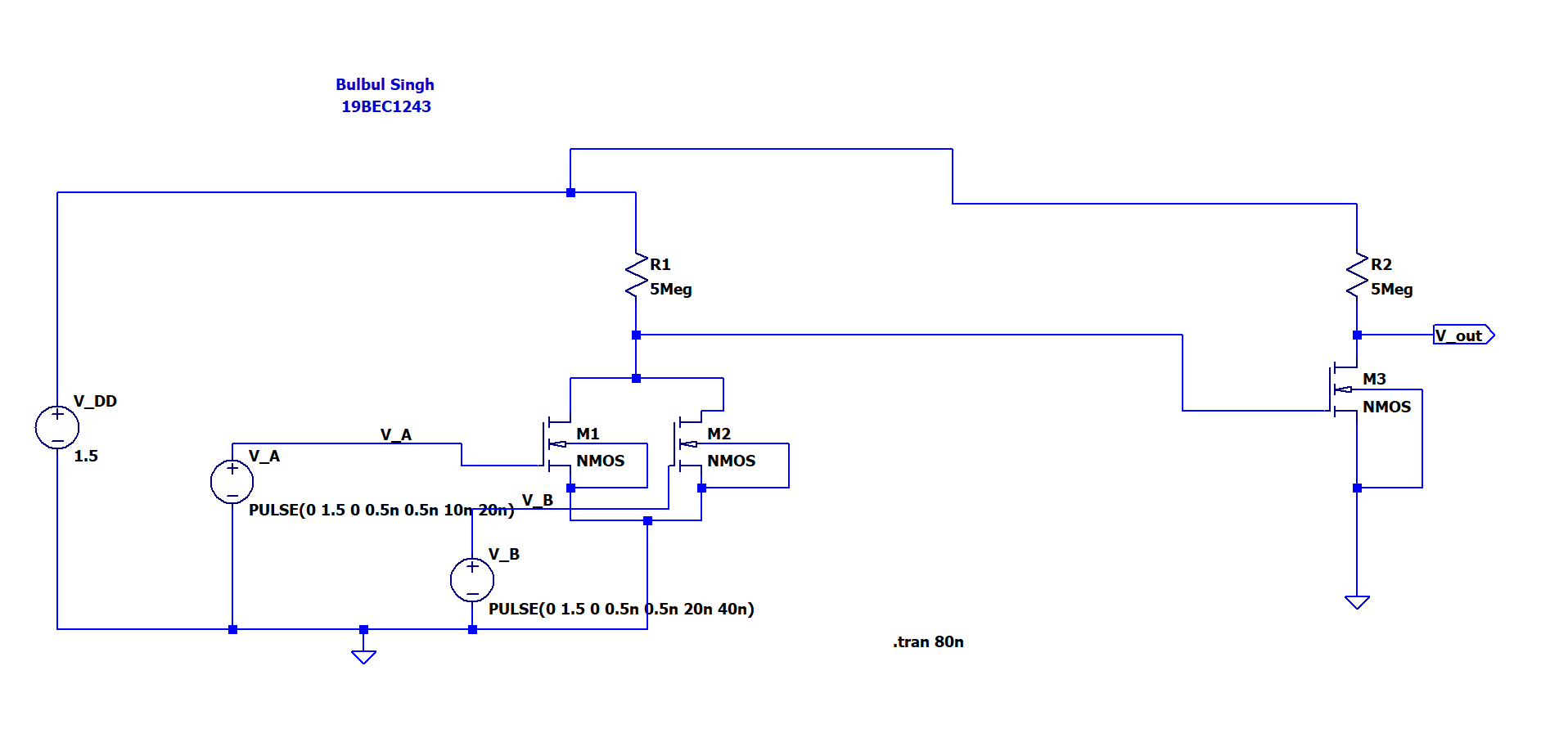
|  |  |  |
| --- | --- | --- |
| **V\_A** | **V\_B** | **V\_out** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Conclusion:**

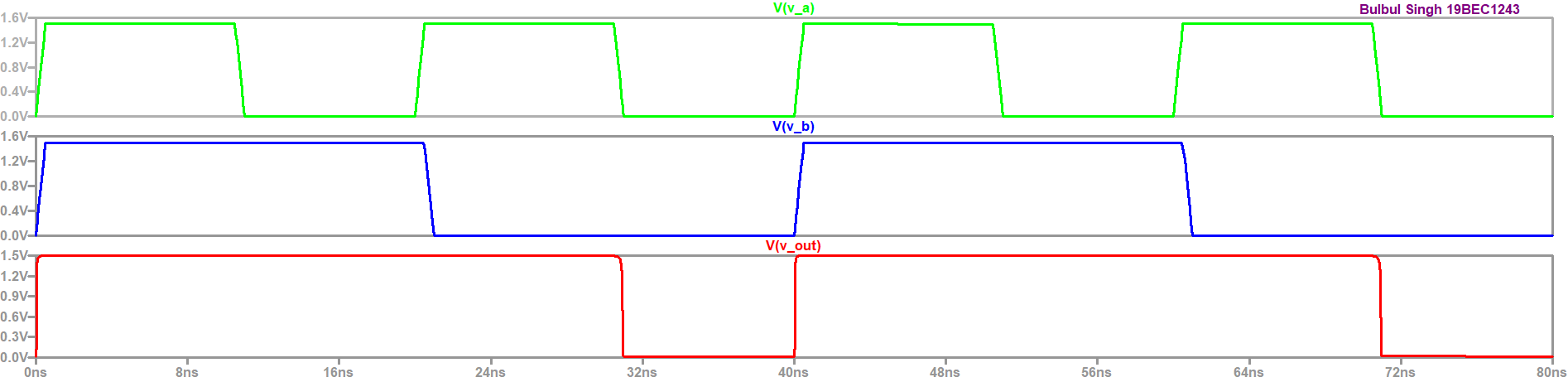
From the graphs of task 3.1 and 3.2 we can observe that when both inputs are low, output is high while in all other cases it is low, this shows the functionality of NOR gate and satisfies the truth table.

**Task 4: OR GATE using NMOS (NMOS4 symbol)**

**Circuit :**

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**Output:**

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**Truth Table:**

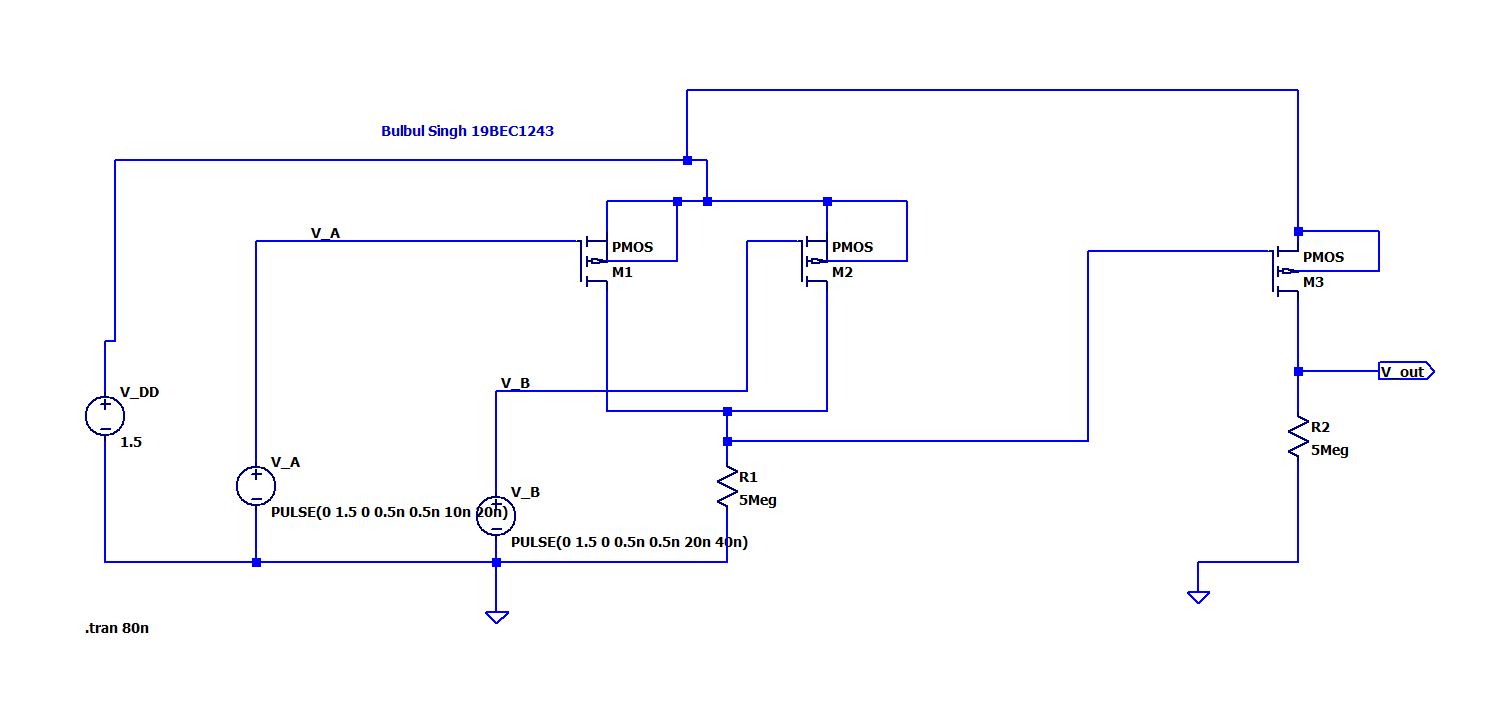
|  |  |  |
| --- | --- | --- |
| **V\_A** | **V\_B** | **V\_out** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Conclusion:**

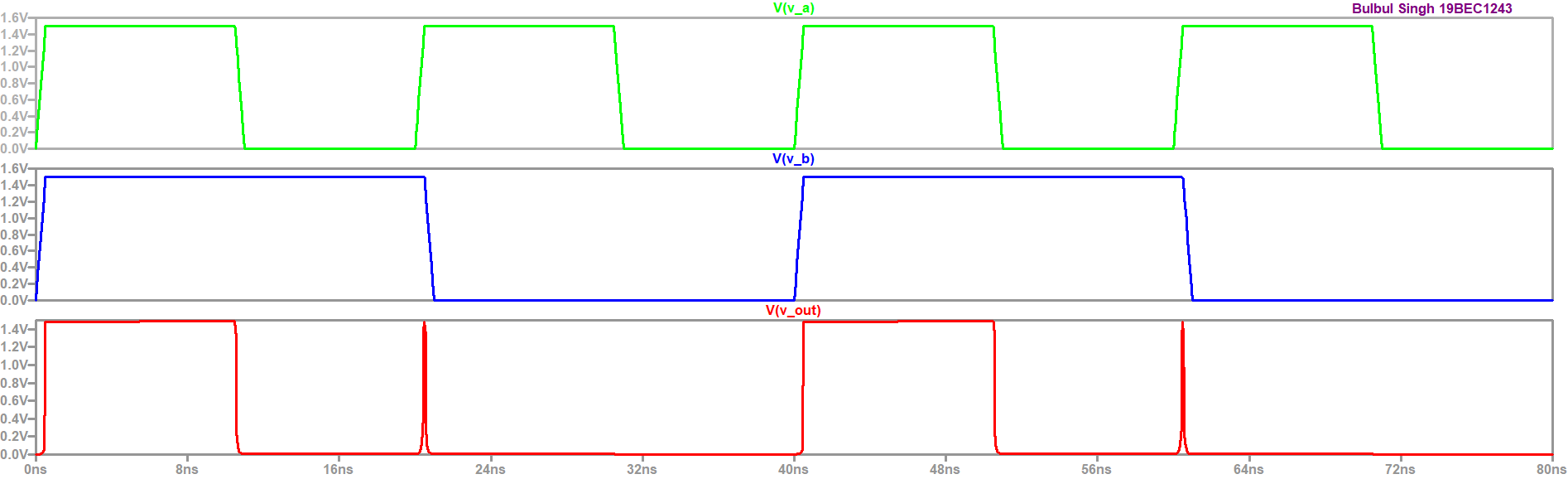
From the graphs of we can observe that when both inputs are low, output is high while in all other cases it is high, this shows the functionality of OR gate and satisfies the truth table.

**Task 5: AND GATE using PMOS(PMOS4 symbol)**

**Circuit:**



**Output:**



**Truth Table:**

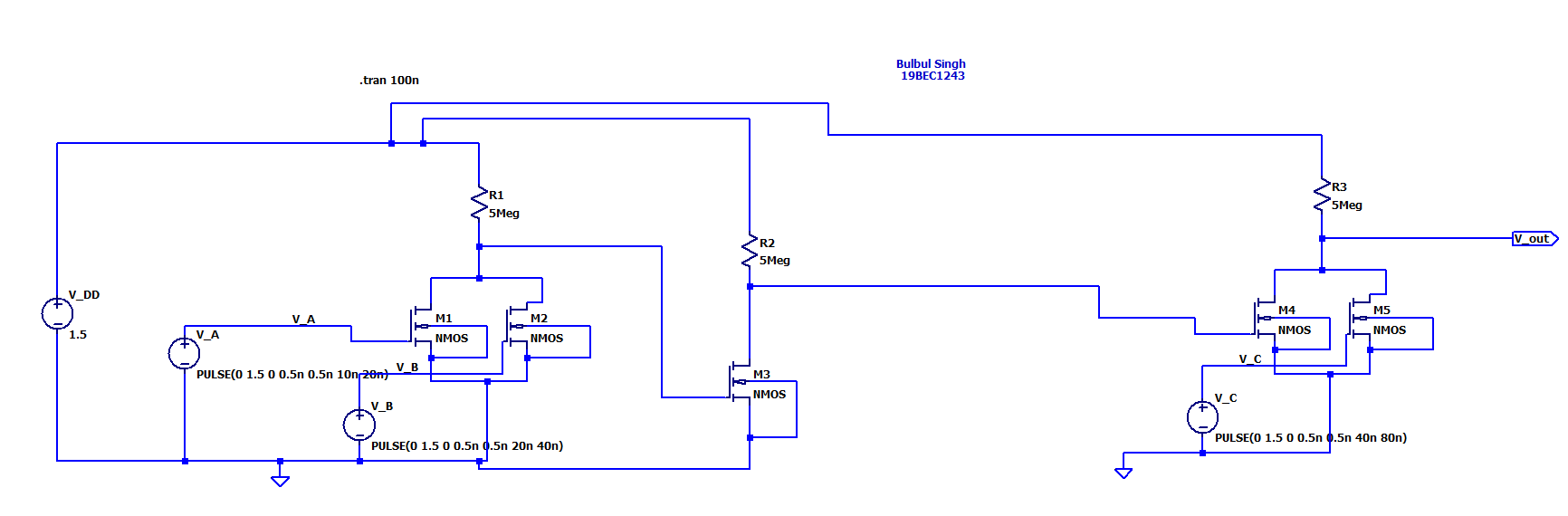
|  |  |  |
| --- | --- | --- |
| **V\_A** | **V\_B** | **V\_out** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Conclusion:**

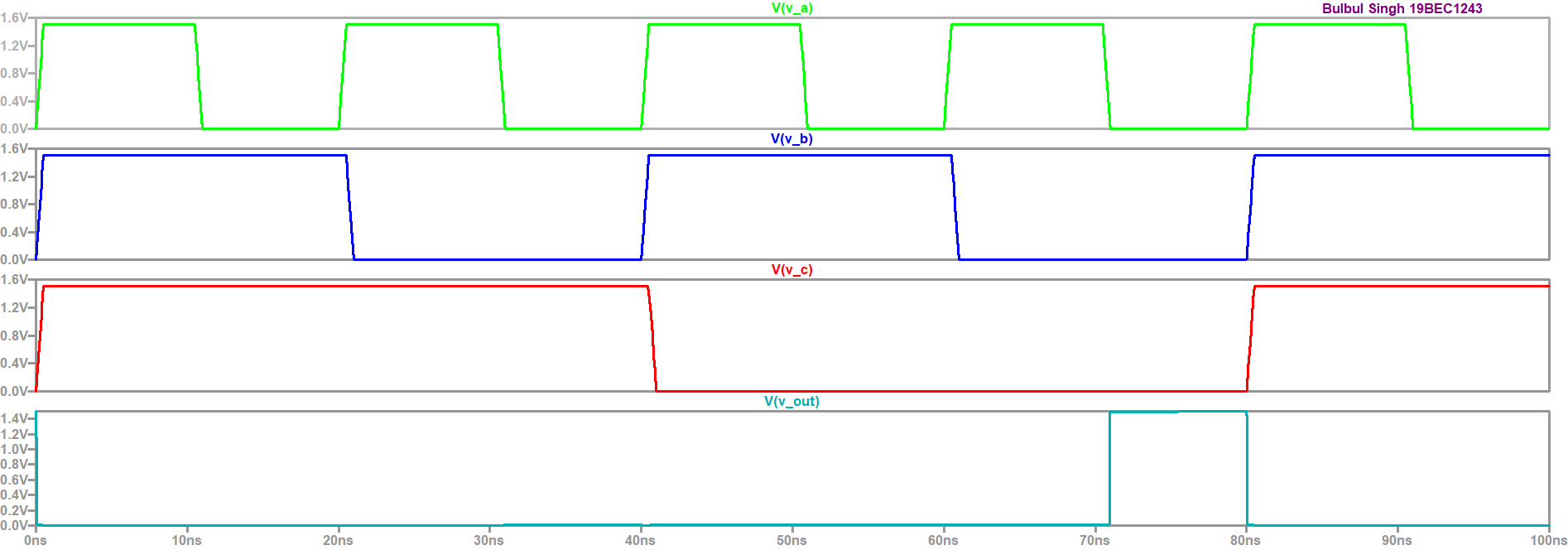
From the graphs of we can observe that when both inputs are high, output is high while in all other cases it is low, this shows the functionality of AND gate and satisfies the truth table.

**Task 6: LOGIC using NMOS(NMOS4 symbol)**

**Circuit:**



**Output:**



**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **V\_A** | **V\_B** | **V\_C** | **V\_out** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Conclusion:**

From the graphs of we can observe that when all three inputs are high, output is high while in all other cases it is low, this shows the functionality of the given Boolean function 𝑌 = 𝐴 + 𝐵 ∙ 𝐶 and satisfies the truth table.